

IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A semiconductor integrated circuit device comprising:

a memory cell array including a memory cell having a ferroelectric capacitor, the memory cell having a first electrode and a second electrode;

a first bit line electrically connected to the first electrode;

a second bit line complementary to the first bit line;

a first potential generation circuit which supplies a first potential to the second electrode to apply a voltage dropping at a first rate of change with a rise of temperature to the ferroelectric capacitor, the first rate of change being equal to dependence on temperature possessed by a saturated voltage of the ferroelectric capacitor; and

a sense amplifier which amplifies a potential difference between the first bit line and the second bit line.

Claim 2 (Canceled).

Claim 3 (Original): The device according to claim 1, further comprising:

a third potential generation circuit supplying a potential which rises at a third rate of change with the rise of temperature as a reference potential to the second bit line.

Claim 4 (Original): The device according to claim 3, wherein the third rate of change is equal to a rate of change, which is dependant on the rise of temperature, of an intermediate value between a maximum value at a "0" data read time from the ferroelectric capacitor and a minimum value at a "1" data read time.

Claim 5 (Currently Amended): ~~The~~ A semiconductor integrated circuit device
~~according to claim 1, wherein comprising:~~

a memory cell array including a memory cell having a ferroelectric capacitor, the
memory cell having a first electrode and a second electrode;

a first bit line electrically connected to the first electrode;

a second bit line complementary to the first bit line;

a first potential generation circuit which supplies a first potential to the second
electrode to apply a voltage dropping at a first rate of change with a rise of temperature to the
ferroelectric capacitor, the first rate of change is being imparted with a dependence on
temperature so that an intermediate value between a maximum value when a "0" data is read
from the ferroelectric capacitor and a minimum value when a "1" data is read is constant
regardless of the temperature; and

a sense amplifier which amplifies a potential difference between the first bit line and
the second bit line.

Claim 6 (Currently Amended): A semiconductor integrated circuit device
comprising:

a memory cell array including a memory cell having a ferroelectric capacitor as a
storage element, the memory cell having a first electrode and a second electrode;

a first bit line electrically connected to the first electrode;

a ~~first~~ second bit line complementary to the first bit line;

a sense amplifier which amplifies a potential difference between the first bit line and
the second bit line; and

a second potential generation circuit supplying a voltage as a power potential of the sense amplifier, the voltage dropping at a second rate of change with a rise of temperature.

Claim 7 (Original): The device according to claim 6, wherein the second rate of change is equal to dependence on temperature possessed by a saturated voltage of the ferroelectric capacitor.

Claim 8 (Original): The device according to claim 6, further comprising:
a third potential generation circuit supplying a potential which rises at a third rate of change with the rise of temperature as a reference potential to the second bit line.

Claim 9 (Original): The device according to claim 8, wherein the third rate of change is equal to a rate of change, which is dependant on the rise of temperature, of an intermediate value between a maximum value at a "0" data read time from the ferroelectric capacitor and a minimum value at a "1" data read time.

Claim 10 (Original): The device according to claim 6, further comprising:
a first potential generation circuit which supplies a first potential to the second electrode to apply a voltage dropping at a first rate of change with the rise of temperature to the ferroelectric capacitor.

Claim 11 (Original): The device according to claim 10, wherein the second rate of change is equal to the first rate of change.

Claim 12 (Original): The device according to claim 10, wherein the first rate of change or the second rate of change is equal to dependence on temperature possessed by a saturated voltage of the ferroelectric capacitor.

Claim 13 (Original): The device according to claim 10, further comprising:
a third potential generation circuit supplying a potential which rises at a third rate of change with the rise of temperature as a reference potential to the second bit line.

Claim 14 (Original): The device according to claim 13, wherein the third rate of change is equal to a rate of change, which is dependant on the rise of temperature, of an intermediate value between a maximum value at a "0" data read time from the ferroelectric capacitor and a minimum value at a "1" data read time.

Claim 15 (Original): The device according to claim 10, wherein the first rate of change is imparted with a dependence on temperature so that an intermediate value between a maximum value when a "0" data is read from the ferroelectric capacitor and a minimum value when a "1" data is read is constant regardless of the temperature.

Claim 16 (Currently Amended): A semiconductor integrated circuit device comprising:

a memory cell array including a memory cell having a ferroelectric capacitor as a storage element, the memory cell having a first electrode and a second electrode;
a first bit line electrically connected to the first electrode;
a second bit line complementary to the first bit line; and

a circuit which supplies a first potential to the second electrode to read information, a time for which the first potential is supplied dropping with a rise of temperature, a dependence on temperature of the time for which the first potential is supplied being equal to that of a time which the polarization of the ferroelectric capacitor needs to reverse.

Claim 17 (Canceled).

Claim 18 (Original): A semiconductor integrated circuit device comprising:
a memory cell array including a memory cell having a ferroelectric capacitor as a storage element, the memory cell having a first electrode and a second electrode;
a first bit line electrically connected to the first electrode;
a second bit line complementary to the first bit line;
a first circuit which supplies a first potential to the second electrode to read information;
a sense amplifier which amplifies a potential difference between the first bit line and the second bit line; and
a second circuit which supplies a second potential as a power potential of the sense amplifier, a time for which the second potential is supplied dropping with a rise of temperature after the first potential is set at a low level.

Claim 19 (Original): The device according to claim 18, wherein a dependence on temperature of the time is equal to that of a time which the polarization of the ferroelectric capacitor needs to reverse.